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HYBRID VIDEO AMPLIFIER CHIP SET FOR HELMET-MOUNTED VISUALLY COUPLED SYSTEMS

Jeff A. Ross

LOGICON TECHNICAL SERVICES, INC.
P.O. BOX 317258
DAYTON, OHIO 45431-7258

Dean Kocian

CREW SYSTEMS DIRECTORATE
HUMAN ENGINEERING DIVISION
WRIGHT-PATTERSON AFB, OHIO 45433-7022

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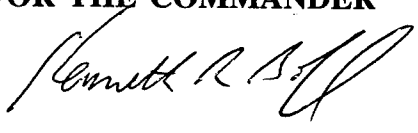

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Jeff A. Ross, P.E.
Dean Kocian

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Logicon Technical Services, Inc.
P.O. Box 317258
Dayton OH 45431-7258

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This paper discusses a new wide-bandwidth Hybrid Video Amplifier Chip Set (HVACS) developed in conjunction with a Quick Disconnect Connector (QDC) with primary application to helmet-mounted displays(HMD). Its major objective is to provide improved control and modulation of the video signal at the cathode ray tube (CRT) while permitting an off-helmet location that places the final video amplification stage much further from the CRT than is the case for direct-view chassis mounted CRTs. The results of this work are being incorporated into a standard pilot-vehicle interface for helmet displays and sights by the Air Force. It is also hoped that this work will lead to an off-the-shelf device for military and industrial applications of helmet displays that utilize helmet-mounted CRT image sources.

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Jeff A. Ross, P.E.
Logicon Technical Services, Inc.
Dayton, Ohio 45433

Dean Kocian
Armstrong Laboratory
Dayton, Ohio 45433

Abstract

This paper discusses a new wide-bandwidth Hybrid Video Amplifier Chip Set (HVACS) developed in conjunction with a Quick Disconnect Connector (QDC) with primary application to helmet mounted displays (HMD). Its major objective is to provide improved control and modulation of the video signal at the cathode ray tube (CRT) while permitting an off-helmet location that places the final video amplification stage much further from the CRT than is the case for direct-view chassis mounted CRTs. The results of this work are being incorporated into a standard pilot-vehicle interface for helmet displays and sights by the Air Force. It is also hoped that this work will lead to an off-the-shelf device for military and industrial applications of helmet displays that utilize helmet-mounted CRT image sources.

Introduction

Background

The proliferation of HMD applications relative to virtual reality and direct information display has led to increased requirements for video performance. A noninterlaced video display format of 1280 x 1024 requires a video bandwidth slightly greater than 100Mhz for proper reproduction of the source video signal. Another requirement stems from the cockpit environment which is subject to high ambient light conditions. This further exacerbates the video HMD design effort in that the CRT may be required to produce several thousand foot-lamberts luminance for adequate display brightness. Therefore, the impact on the video amplification electronics is a dual requirement of wide bandwidth at large voltage swing. This particular signal profile requirement is common to essentially all direct-view, projection, and helmet mounted displays. However, unique to the HMD is the problem of how to provide this CRT drive capability to the electrodes of the CRT when the CRT is mounted in the helmet. There has been considerable effort over the years to develop HMD technology with a variety of configurations used to provide the required high performance video signal to the CRTs. The location of the final video amplification stage has been a subject given considerable attention relative to the associated tradeoffs.

Objective

The primary objective of this effort was to develop a hybrid integrated circuit chip set capable of providing the necessary video drive envelop for CRT configured helmet systems displaying either stroke symbology or raster imagery/symbology while permitting an off-helmet location for the drive electronics. A secondary objective was to produce a signal transmission and packaging concept that would be compatible with a standardized pilot-vehicle interface comprising a ground egress and ejection-capable, high-voltage, quick-disconnect connector, and wiring harness system.

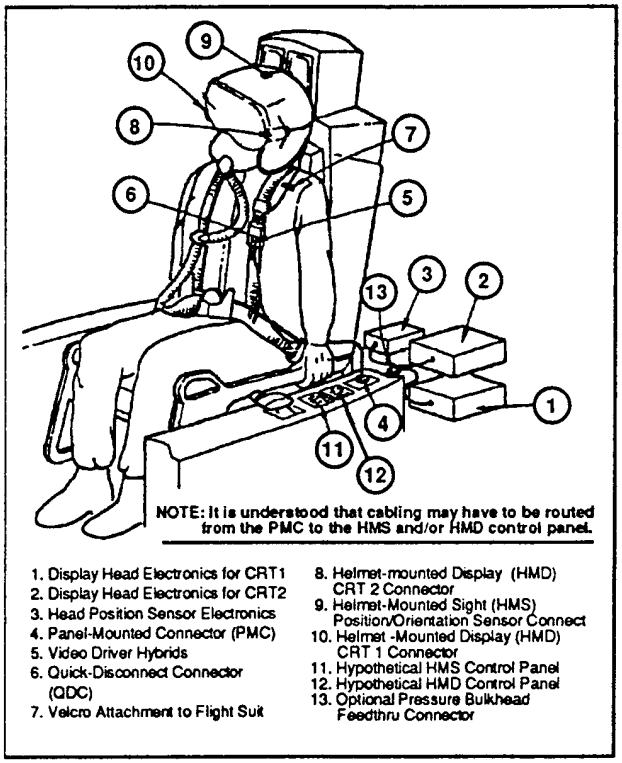

Figure 1 - QDC/HVACS System Configuration

System Configuration

Quick-Disconnect Connector

Figure 1 depicts the basic system concept for the QDC and its associated wiring harness. The University of

Dayton Research Institute (UDRI) was selected to provide the mechanical and thermal design of the QDC and Reynolds Industries Incorporated was selected to implement the QDC and wiring harness design. The QDC-specific wiring harness is considered to run from its mating interface to the helmet mounted CRTs and helmet sight sensor, denoted as positions 8, 9 and 10, to its mating interface with the panel mounted connector (PMC) denoted as position 4. In addition to providing a standardized interface, the primary functions of the QDC and wiring harness assembly are to provide arc-free disconnects during ground egress in explosive vapor environments, facilitate separation during aircraft ejections, provide compatible transport of high voltage power and wideband video signals to the helmet and low-noise low level signals from the helmet to aircraft electronics. The current version of the QDC provides 8 high voltage and 54 signal leads to support a binocular helmet display with 2 CRTs and a helmet tracker system. System serial read only memories (ROMs) are used for CRT and helmet mounted sensor (HMS) characterizations.

CRTs used for high performance video applications normally have the final video signal amplification stage mounted within a few inches of the CRT. This type of circuit topology minimizes the signal performance degrading effects associated with stray and load capacitance as well as electromagnetic and radio interference (EMI/RFI). As shown in the circuit analysis portion of this paper, among the most important system design issues is the location of the video amplifier portion of the HVACS. Referring again to Figure 1, at least 4 locations might be hypothesized for the location of the video amplifier. These potential locations are at the helmet, just off the helmet, in the QDC, or at the panel. A helmet mounted location near the CRT is ideal for ensuring maximum signal bandwidth and minimum signal noise. However, this choice only exacerbates critical helmet weight and thermal design considerations associated with most VCS configurations. A mounting location just off the helmet is not compatible with most VCS configurations. It presents possibilities for interference with the ejection seat pitot tube air flow and parachute riser line deployment. A panel mounted location requires a long transmission line and presents increased susceptibility to the signal degrading effects of distributed capacitance and EMI/RFI. Therefore, a mounting location in the aircraft side of the QDC, as shown in Figure 2, was selected for this effort because it offers a reasonable set of compromises for signal bandwidth, signal integrity, thermal cooling, and operational safety.

Video Processor Hybrid

M.S. Kennedy Corporation was selected to hybridize the video processor and video amplifier circuit designs. The video processor hybrid (ALVP100) is comprised of the circuits which provide low-level video signal gain, contrast adjust, blanking, black level clamp, and DC bias. Figure 3 shows the block diagram for the ALVP100.

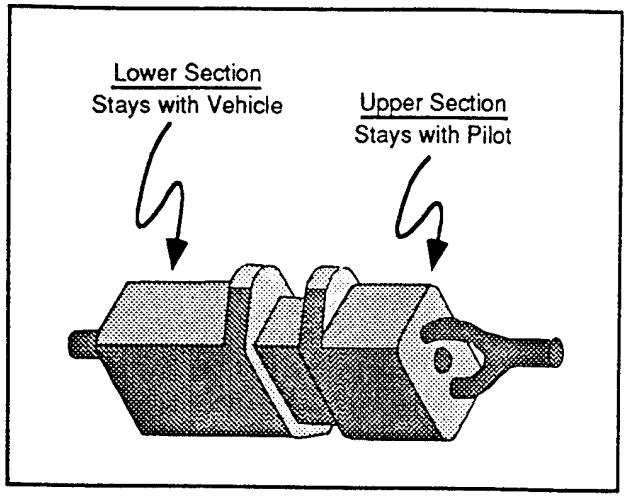

Figure 2 - Quick-Disconnect Connector

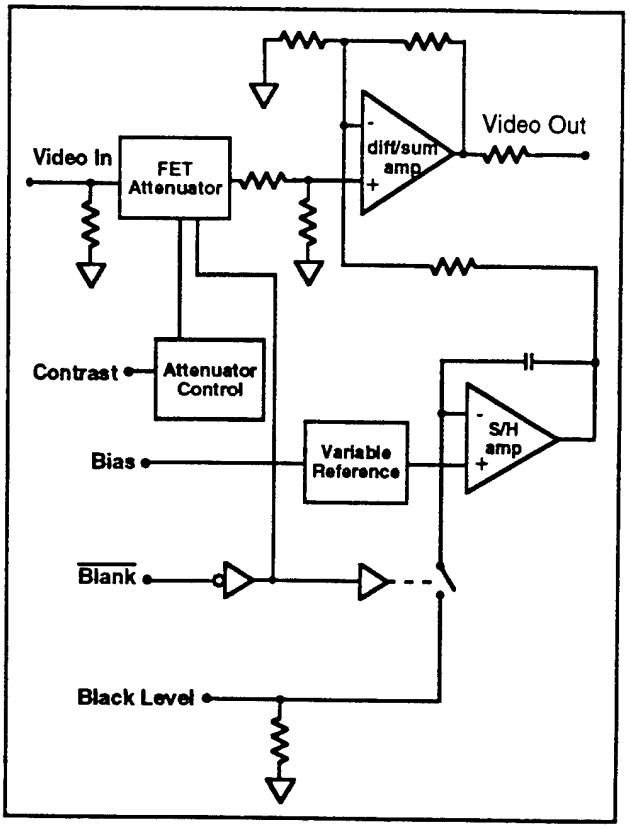

Figure 3 - Video Processor Hybrid

Integral to the wideband performance of this hybrid is a Comlinear CLC404 current-feedback differential amplifier integrated circuit (IC) that has a nominal frequency response of 165Mhz and the capability to drive a 75 ohm line. This device is used as a differential/summing amplifier to process the video and black level signals. The contrast function is achieved by a "T" configured DC controlled MOSFET attenuator circuit. Low capacitance Siliconix SD210 MOSFETs are used in the attenuator to minimize amplitude reduction versus frequency.

Stable DC performance of the ALVP100 is achieved by the black level clamp circuit which is an LF156A FET-input operational amplifier IC configured as a sample and hold amplifier. A sample of the video amplifier DC output voltage is taken during the blanking interval. This clamp circuit provides a DC correction voltage to the differential/summing amplifier during active video which DC stabilizes the video processor and video amplifier loop. A bias adjustment signal provides a DC offset voltage to enable alignment of the video signal and, thus, ensure linear operation of the video amplifier hybrid.

The video processor and video amplifier hybrid packages are shown in Figure 4. An 18 pin TUB that measures approximately 0.975" x 0.775" x 0.190" (l x w x h) houses the video processor circuit. The nominal power dissipation is approximately 1.0W.

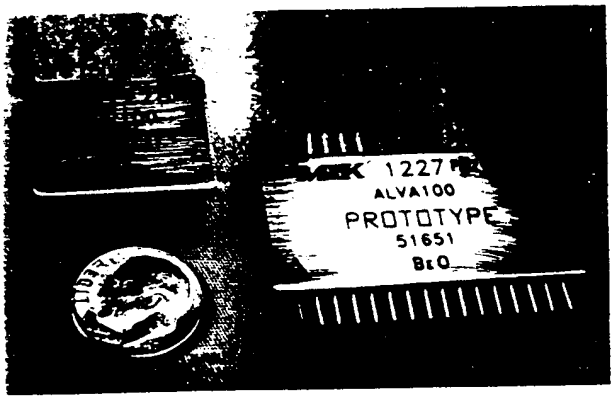

Figure 4 - HVACS Packages

Video Amplifier Hybrid

Figure 5 is a block diagram of the video amplifier hybrid (ALVA100). The device is designed to provide cathode video modulation and grid1 (G1) DC bias to the CRT. An important reason for selecting cathode drive versus differential drive is that dual electrode drive affects the G1/G2 crossover point setting leading to undesirable spot size conditions [1, 2]. Also, differential drive circuits are susceptible to response time differences which may become significant at higher operating frequencies. The amplifier drive challenge has been to design the drive electronics to provide the required wideband voltage swing to ensure a high brightness and high resolution CRT display. CRT manufacturers such as Hughes Display Products may consider as a design goal a cutoff potential of about 70V to 80V with a full luminance drive capability approaching 50V.

The drive envelop is achieved by a buffered cascode amplifier design which provides a frequency response of greater than 100Mhz at voltage swings up to 50V into an 8.0pf load [3]. Excellent swing and response performance is obtained by using the Motorola MRF544/545 series bipolar transistors for the amplifier.

G1 bias is provided by a Harris HA2525 high speed operational amplifier IC controlling a high voltage bipolar transistor to achieve an extended DC range from 5V to -50V. The +60V output from the cathode amplifier and the -50V output from the G1 amplifier provide a maximum CRT cutoff voltage approaching 110V. A CRT phosphor protect function is achieved by an active switch used to clamp the G1 amplifier control voltage to 0V which causes the output of the G1 amplifier to be pulled to -50V during system failures.

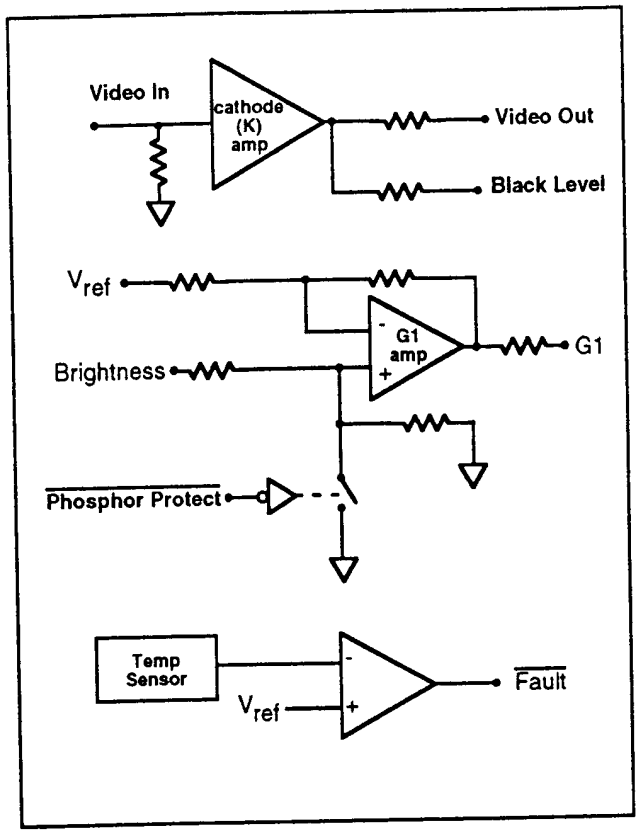

Figure 5 - Video Amplifier Hybrid

The LM135 precision temperature sensor IC is used to monitor the substrate temperature of the ALVA100. It generates a DC voltage which changes at the rate of approximately 10mV/°C. This voltage is compared to a fixed reference voltage through an LM111 linear comparator IC to generate a temperature fault signal when approximately 90% (135°C) of the active component maximum junction temperature is exceeded. Refer to Figure 4 for the video amplifier hybrid package. The package is a power pack measuring about 1.5" x 1.0" x 0.2" and has a nominal power consumption of about 6.7W at a video modulation of 70%.

System Performance

Pulse Response

A primary performance concern associated with the HVACS as a system is its increased pulse response time as a function of cable, stray, and load capacitance. Table 1 shows equivalent bandwidths for various cable lengths and load capacitances. A transmission line may be modeled as

a series of low pass filters per unit length that progressively attenuate the transmitted signal [4]. Pulse response tests were performed using an evaluation printed circuit board, various lengths of 95 ohm Cheminax #9530H1014 coaxial cable, and various load capacitances. A HP8082A pulse generator and TEK2465B oscilloscope were used to evaluate response time performance. The output response times were adjusted by square-root-sum-of-squares to eliminate source input response. Resultant response times were converted to an equivalent first-order bandwidth. Load capacitance consists of FET probe, CRT equivalent, and estimated stray capacitances. Figure 6 shows the HVACS pulse response at the end of four feet of cable with C(load) of 4.5pf. The equivalent bandwidth of this response is about 100 Mhz.

Cable Length	Load Capacitance	Equivalent Bandwidth
6 feet	3.5 pF	94.7 MHz
6 feet	6.5 pF	92.2 MHz
10 feet	3.5 pF	85.1 MHz
10 feet	6.5 pF	80.4 MHz

Table 1 - Equivalent Bandwidths

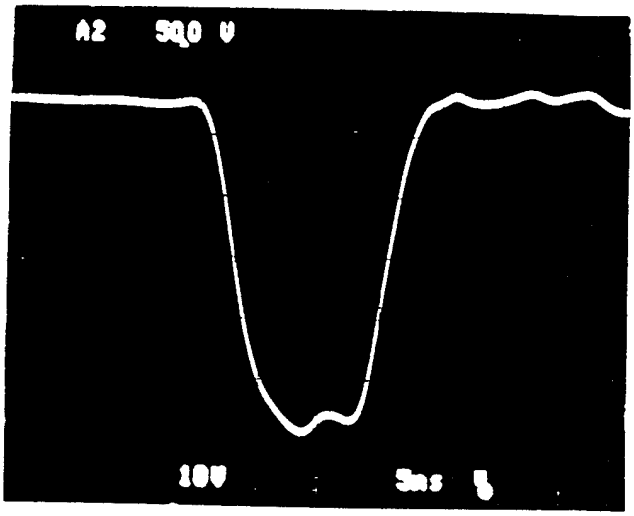

Figure 6 - Pulse Response

Frequency Response

Figure 7 shows the sweep frequency response of the HVACS. This test was performed at an output voltage swing of 50Vpp using a HP3577B network analyzer. Again the output measurement was made at the end of four feet of cable with a load capacitance of 4.5pf. Table 2 shows the salient performance specifications of the HVACS.

Conclusion

The HVACS provides a 100Mhz capability for unterminated cable lengths of up to four feet and nominal CRT electrode capacitances. Also, modulation capability provides ample CRT drive to meet high brightness requirements for HMDs. The QDC system provides an effective means of signal-to-CRT interface while ensuring pilot ease of use and safety upon ejection. Display resolution and brightness objectives are maintained through the integrated approach of the HVACS and QDC.

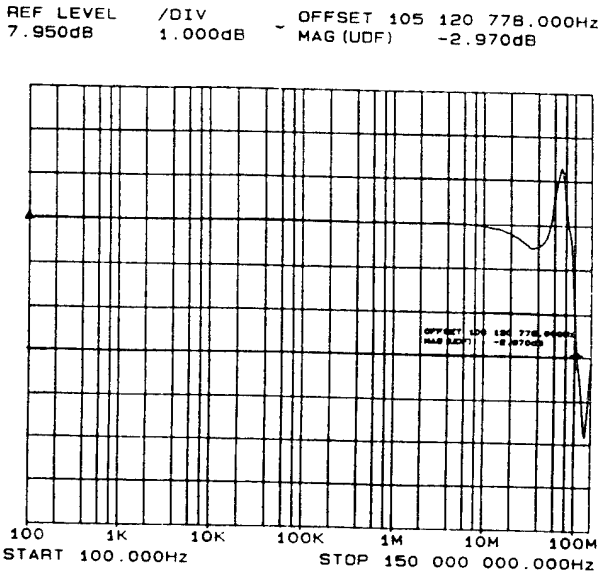

Figure 7 - Frequency Response

Device	Frequency Response (-3dB)	Gain Flatness (≤70 MHz)	Step Response (10%-90%)	Voltage Swing
ALVP100	150.0 MHz	± 1.0 dB	2.33 ns	3.0 V_{p-p}
ALVA100 K Amp	100.0 MHz	± 1.0 dB	3.50 ns	50.0 V_{p-p}
G1 Amp	350.0 KHz	----------	1000.0 ns	55.0 V_{p-p}

Table 2 - Hybrid Specifications

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